WHAT IS CLAIMED IS:

1. A semiconductor topography, comprising:

a silicon dioxide layer with a thickness equal to or less than approximately 10 angstroms; and

a silicon nitride layer arranged upon and in contact with the silicon dioxide layer.

2. The semiconductor topography of claim 1, wherein said thickness of the silicon dioxide layer is between approximately 6 angstroms and approximately 10 angstroms.

3. The semiconductor topography of claim 1, wherein said silicon nitride layer comprises a thickness greater than approximately 15 angstroms.

4. The semiconductor topography of claim 1, wherein said silicon dioxide layer is arranged upon and in contact with a silicon-based semiconductor substrate.

5. The semiconductor topography of claim 1, wherein said silicon dioxide layer is arranged upon and in contact with a polysilicon layer.

6. A semiconductor device comprising an oxide-nitride gate dielectric having substantially similar gate to substrate capacitance as an oxide gate dielectric comprising a thickness less than approximately 20 angstroms.

7. The semiconductor device of claim 6, wherein said oxide-nitride gate dielectric has a substantially similar gate to substrate capacitance as an oxide gate dielectric having a thickness between approximately 10 angstroms and approximately 15 angstroms.

8. The semiconductor device of claim 6, wherein said oxide-nitride gate dielectric comprises an oxide thickness between approximately 6 angstroms and approximately 10 angstroms and a nitride thickness between approximately 15 angstroms and approximately 20 angstroms.

9. The semiconductor device of claim 6, wherein said oxide-nitride gate dielectric comprises a thickness that varies by less than approximately 5% across the semiconductor topography.

10. The semiconductor device of claim 6, wherein said oxide-nitride gate dielectric comprises a greater density than said oxide gate dielectric.

11. The semiconductor device of claim 6, wherein said oxide-nitride gate dielectric comprises fewer defects than said oxide gate dielectric.

12. A method for processing a semiconductor topography, comprising:

growing an oxide film upon the semiconductor topography in the presence of an ozonated substance; and

depositing a silicon nitride film upon and in contact with the oxide film.

13. The method of claim 12, wherein said ozonated substance comprises ozonated deionized water.

14. The method of claim 12, wherein said ozonated substance comprises ozonated deuterium oxide.

15. The method of claim 12, wherein said ozonated substance comprises an ozone concentration between approximately 20 ppm and approximately 50 ppm.

16. The method of claim 13, further comprising annealing the semiconductor topography subsequent to said depositing the silicon nitride film.

17. The method of claim 16, wherein said annealing comprises exposing the semiconductor topography to ammonia or nitrous oxide.

18. The method of claim 16, wherein said annealing comprises exposing the semiconductor topography to deuterium ammonia.

19. A method for forming an oxide-nitride stack, comprising:

growing an oxide film in a first chamber at a first temperature;

transferring the semiconductor topography from said first chamber to a second chamber, wherein said transferring comprises exposing the semiconductor topography to a substantially similar temperature as said first temperature; and

forming a nitride layer upon the oxide film in said second chamber at a second temperature.

20. The method of claim 19, wherein said first temperature is between approximately 10 °C and approximately 30 °C.

21. The method of claim 19, wherein said second temperature is between approximately 750 °C and approximately 800 °C.

22. The method of claim 19, wherein said growing comprises rinsing the semiconductor topography with an ozonated substance.

23. The method of claim 19, further comprising annealing said semiconductor topography at a third temperature subsequent to said forming the nitride layer.

24. The method of claim 23, wherein said third temperature is between approximately 750 °C and approximately 850 °C.

25. The method of claim 19, further comprising forming a second oxide film upon and in contact with the nitride film at a fourth temperature, wherein said fourth temperature is greater than the first temperature.